REMARKS

Claims 7-12 stand rejected under 35 USC §101 as being directed to non-statutory subject matter. Claims 1-18 stand rejected under 35 USC §102(b) as being anticipated by Yuan et al., U.S. patent 6,321,186.

Claims 1, 7, and 13 have been amended to more clearly state the invention.

Claim 7 has been amended to accommodate the Examiner's rejection under 35 USC §101. As amended, claim 7 recites that the computer readable medium including instructions stored on a computer readable medium, wherein said instructions, when executed by the computer system cause the computer system to perform the steps of. Thus, independent claim 7, as amended, is believed to clearly recite statutory subject matter. Reconsideration and withdrawal of the rejection of claims 7-12 under 35 USC §101 is respectfully requested.

Reconsideration and allowance of the pending claims 1-18, as amended, is respectfully requested.

Yuan et al., U.S. patent 6,321,186 discloses a method for verifying an integrated circuit design using constraint information to develop a weighted data structure. In one embodiment, a binary decision diagram (BDD) includes a plurality of nodes (401, 402, 403, 404, 405, 406, 407, 420, and 430) representing signals and states in the circuit, and each node has a branching probability based on user-defined weights. The BDD represents the intersection of the input space and state space which satisfies the constraints. Current state information resulting from simulation is used to

dynamically adjust the branching probabilities of the BDD on the fly. In one embodiment, the constraint information is applicable for formal verification of a portion of the circuit. In another embodiment, a simulation controller (12) receives design and constraint information and generates the program to control simulator (14).

Applicants respectfully submit that each of the independent claims 1, 7, and 13, as amended, is patentable over the references of record including Yuan et al. Independent claims 1, 7, and 13, as amended, recite a method, a computer program product, and apparatus for implementing a level bias function, or an operand level bias, for branch prediction control for generating test simulation vectors. In the present invention, as illustrated and described in the specification, a level bias function function134 enables reliably predicting whether or not a branch will be taken, in all test cases, and the need to rely on any hard coded values as used in the past is eliminated.

Each of the independent claims 1, 7, and 13, as amended, is believed to be in condition for allowance. Reconsideration and withdrawal of the rejection of claims 1-18 under 35 USC §112, second paragraph, and of claims 7-12 under 35 USC §101 is respectfully requested.

Dependent claims 2-6, 8-12, and 14-18 further define the invention of patentable claims 1, 7, and 13, and are likewise patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance

and allowance of each of the pending claims 1-18, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

S-signature by

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